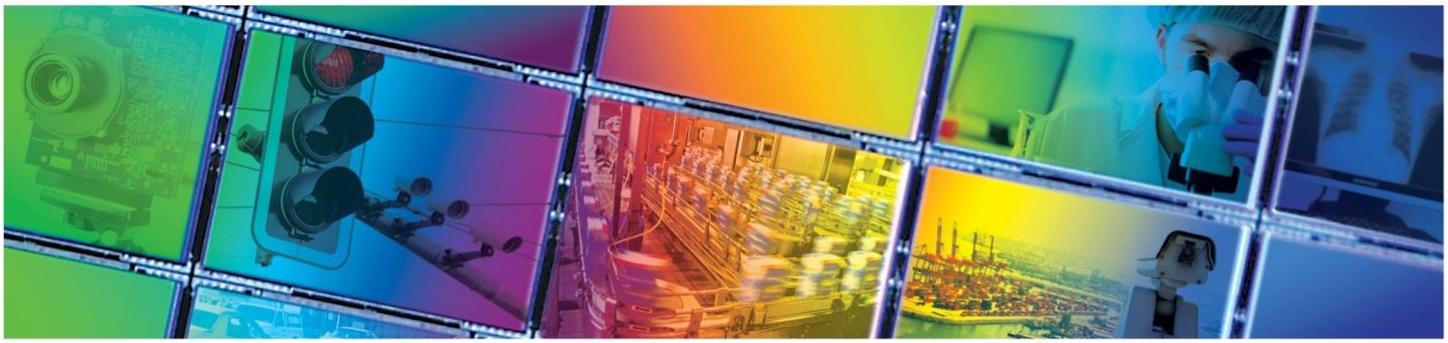
TRUESENSE
imaging, inc.

KAF-16801 IMAGE SENSOR

4096 (H) X 4096 (V) FULL FRAME CCD IMAGE SENSOR



JULY 20, 2012

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.0 PS-0032

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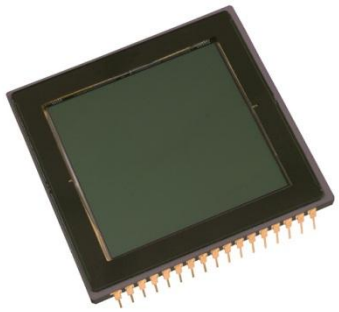
KAF-16801 Image Sensor



DESCRIPTION

The KAF-16801 is a high performance area CCD (charge-coupled device) image sensor with 4096 H x 4096 V photo active pixels designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

FEATURES

- True Two Phase Full Frame Architecture
- TRUESENSE Transparent Gate Electrode for high sensitivity
- 70% Fill Factor with anti-blooming drain
- Low Dark Current
- High Output Sensitivity

APPLICATION

- Scientific Imaging

Parameter	Typical Value
Architecture	Full Frame CCD
Pixel Count	4096 (H) x 4096 (V)
Pixel Size	9 µm (H) x 9 µm (V)
Imager Size	36.88 mm (H) x 36.88 mm (V)
Chip Size	38.60 mm (H) x 37.76 mm (V)
Optical Fill Factor	100%
Saturation Signal	100,000 electrons
Output Sensitivity	13 µV/electron
Dark Current (25 °C, Accumulation Model)	<10 pA/cm^2
Dark Current Doubling Rate	6 °C
Dynamic Range (Saturation Signal/Dark Noise)	76 dB
Quantum Efficiency (450, 550, 650 nm)	40%, 52%, 65%
Maximum Data Rate	10 MHz
Package	CERDIP Package (sidebrazed)
Cover Glass	Clear

Note: All values measured at 25 °C.

Ordering Information

Catalog Number	Product Name	Description	Marking Code
2H4793	KAF-16801-AAA-DP-B1	Monochrome, No Microlens, CERDIP Package (sidebrazed, CuW), Taped Clear Cover Glass, No Coatings, Grade 1	KAF-16801-AAA (Serial Number)
2H4794	KAF-16801-AAA-DP-B2	Monochrome, No Microlens, CERDIP Package (sidebrazed, CuW), Taped Clear Cover Glass, No Coatings, Grade 2	
2H4798	KAF-16801-AAA-DP-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed, CuW), Taped Clear Cover Glass, No Coatings, Engineering Sample	
4H0082	KEK-4H0082-KAF-16801-12-5	Evaluation Board (Complete Kit)	N/A

See Application Note *Product Naming Convention* for a full description of the naming convention used for Truesense Imaging image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

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Rochester, New York 14615

Phone: (585) 784-5500
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Truesense Imaging reserves the right to change any information contained herein without notice. All information furnished by Truesense Imaging is believed to be accurate.

Device Description

ARCHITECTURE

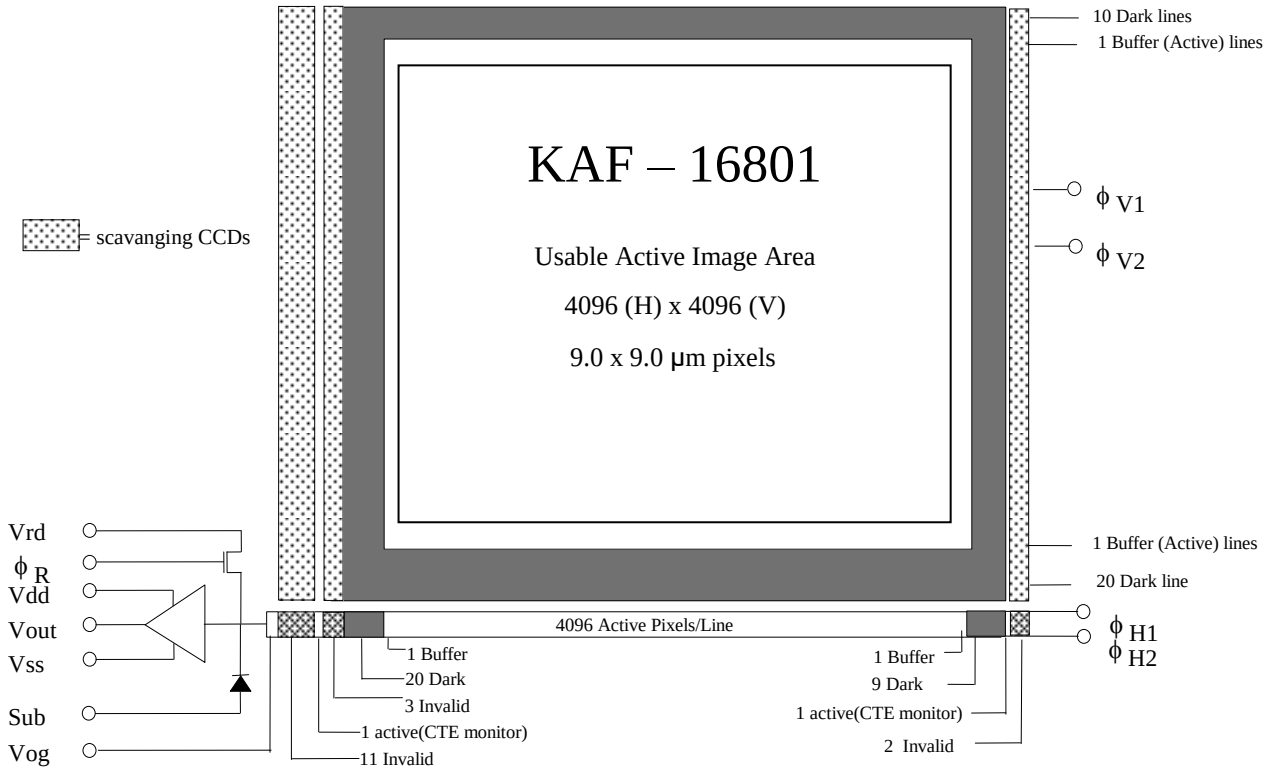


Figure 1: Block Diagram

The sensor consists of 4127 parallel (vertical) CCD shift registers each 4128 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The elements of these registers are arranged into a 4096 x 4096 photosensitive array surrounded by a light shielded dark reference of 29 columns and 30 rows. There is a buffer region of one photosensitive pixel surrounding the photosensitive region (one column at the beginning of a line, one column at the end of a line, one row at the beginning of a frame, and one row at the end of a frame). The parallel (vertical) CCD registers transfer the image one line at a time into a single 4145 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a three-stage source follower that converts the photo-generated charge to a voltage for each pixel.

Dark Reference Pixels

Surrounding the peripheral of the device is a border of light shielded pixels. This includes 20 leading and 10 trailing pixels on every line excluding the inactive and photosensitive buffer pixels. There are also 20 full dark lines at the start of every frame and 10 full dark lines at the end of each frame. Under normal circumstances, these dark reference pixels do not respond to light. However, the pixels in close proximity to an active pixel, or the outer bounds of the can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD. Once the signal has been sampled by the system electronics, the reset gate (φR) is clocked to remove the signal and FD is reset to the potential applied by Vrd. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device – see Figure 2.

Transfer Efficiency Test Pixels and Dummy Pixels

At the beginning of each line and at the end of each line are extra horizontal CCD pixels. These are a combination of pixels that are not associated with any vertical CCD register and two that are associated with extra photo active vertical CCDs. The two extra photo active vertical CCDs are provided to give an accurate photo generated signal that can be used to monitor the charge transfer efficiency in the serial (horizontal) register.

They are arranged as follows beginning with the first pixel in each line

- 11 dark, inactive pixels
- 1 photo active test pixel
- 3 inactive pixels
- 20 dark reference pixels
- 1 active buffer pixel
- 4096 photoactive pixels
- 1 active buffer pixel
- 9 dark reference pixels
- 1 photoactive test pixel
- 2 inactive pixels

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the φV1 and φV2 register clocks are held at a constant (low) level. See Figure 7.

Charge Transport

Referring again to Figure 7 - Timing Diagrams, the integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCDs to the horizontal CCD register using the φV1 and φV2 register clocks. The horizontal CCD is presented a new line on the falling edge of φV1 while φH2 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the φH1 and φH2 pins in a complementary fashion. On each falling edge of φH1 a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

HORIZONTAL REGISTER

Output Structure

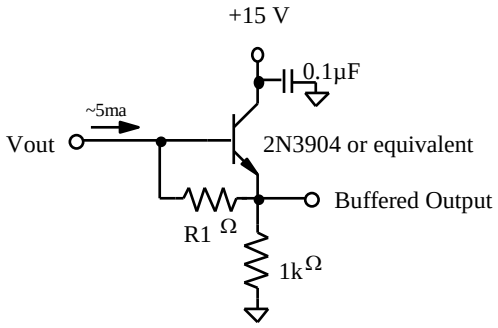


Figure 2: Output Structure Load Diagram

Notes:

1. For operation of up to 10 MHz.
2. The value of R1 depends on the desired output current according the following formula: R1 = 0.7 / Iout.
3. The optimal output current depends on the capacitance that needs to be driven by the amplifier and the bandwidth required. 5 mA is recommended for capacitance of 12 pF and pixel rates up to 20 MHz.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

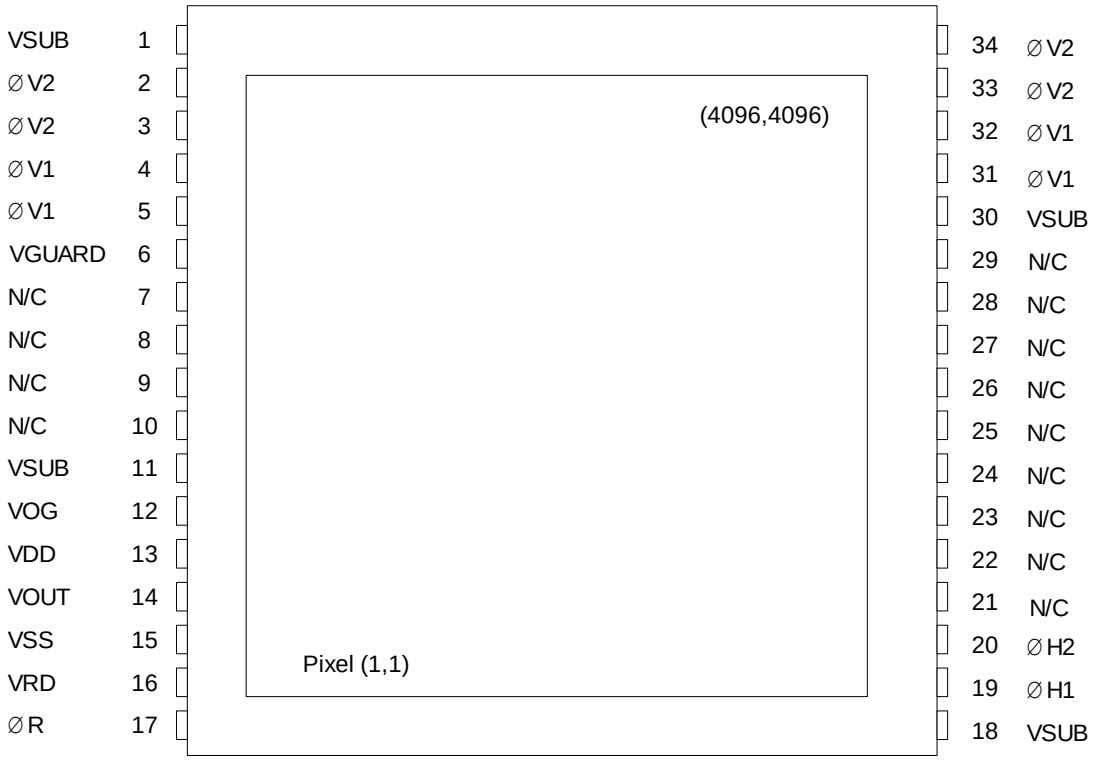


Figure 3: Pinout Diagram

Pin	Name	Description
1	VSUB	Substrate (Ground)
2	φV2	Vertical CCD Clock - Phase 2
3	φV2	Vertical CCD Clock - Phase 2
4	φV1	Vertical CCD Clock - Phase 1
5	φV1	Vertical CCD Clock - Phase 1
6	VGUARD	Guard Ring
7	N/C	No Connection (open pin)
8	N/C	No Connection (open pin)
9	N/C	No Connection (open pin)
10	N/C	No Connection (open pin)
11	VSUB	Substrate (Ground)
12	VOG	Output Gate
13	VDD	Amplifier Supply
14	VOUT	Video Output
15	VSS	Amplifier Supply Return
16	VRD	Reset Drain
17	φR	Reset Clock

Pin	Name	Description
34	φV2	Vertical CCD Clock - Phase 2
33	φV2	Vertical CCD Clock - Phase 2
32	φV1	Vertical CCD Clock - Phase 1
31	φV1	Vertical CCD Clock - Phase 1
30	VSUB	Substrate (Ground)
29	N/C	No Connection (open pin)
28	N/C	No Connection (open pin)
27	N/C	No Connection (open pin)
26	N/C	No Connection (open pin)
25	N/C	No Connection (open pin)
24	N/C	No Connection (open pin)
23	N/C	No Connection (open pin)
22	N/C	No Connection (open pin)
21	N/C	No Connection (open pin)
20	φH2	Horizontal CCD Clock - Phase 2
19	φH1	Horizontal CCD Clock - Phase 1
18	VSUB	Substrate (Ground)

Imaging Performance

Typical Operational Conditions

All values measured at 25 °C, and nominal operating conditions. These parameters exclude defective pixels.

Specifications

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes	Verification Plan
Saturation Signal Vertical CCD Capacity Horizontal CCD Capacity Output Node Capacity	Nsat	90000	 100000 200000 180000	 120000 250000	electrons /pixel	1	design[12]
Photoresponse Non-Linearity	PRNL		1	2	%	2	design[12]
Photoresponse Non-Uniformity	PRNU		1	3	%	3, 10	die[11]
Dark Signal	Jdark		18 3.5	50 10	electrons / pixel / sec pA/cm^2	4	die[11]
Dark Signal Doubling Temperature		5	6.3	7.5	°C		design[12]
Dark Signal Non-Uniformity	DSNU		18	50	electrons / pixel / sec	5, 10	die[11]
Dynamic Range	DR	73	76		dB	6	design[12]
Charge Transfer Efficiency	CTE	0.99997	0.99999				die[11]
Output Amplifier DC Offset	Vodc	Vrd-3	Vrd-2.5	Vrd-2	V	7	die[11]
Output Amplifier Bandwidth	f-3dB		140		Mhz	8	design[12]
Output Amplifier Sensitivity	Vout/Ne$^-$	12.5	13	14	µV/e$^-$		design[12]
Output Amplifier Output Impedance	Zout		130		Ohms		design[12]
Noise Floor	ne$^-$		15	20	electrons	9	die[11]

Notes:

1. For pixel binning applications, electron capacity up to 270,000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
2. Worst case deviation from straight line fit, between 1% and 90% of Vsat.
3. One Sigma deviation of a 128 x 128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25 °C.
5. Average dark signal of any of 32 x 32 blocks within the sensor. (each block is 128 x 128 pixels)
6. 20log (Nsat / ne^-) at nominal operating frequency and 25 °C.
7. Video level offset with respect to ground
8. Assumes 10 pF off-chip load.
9. Output amplifier noise at 25 °C, operating at pixel frequency up to 2 MHz, bandwidth = 20 MHz, tint = 0, and no dark current shot noise.
10. Specification excludes region [1, 1, 400, 400]. See Dark Current Nonuniformity.
11. A parameter that is measured on every sensor during production testing.
12. A parameter that is quantified during the design verification activity.

Typical Peformance Curves

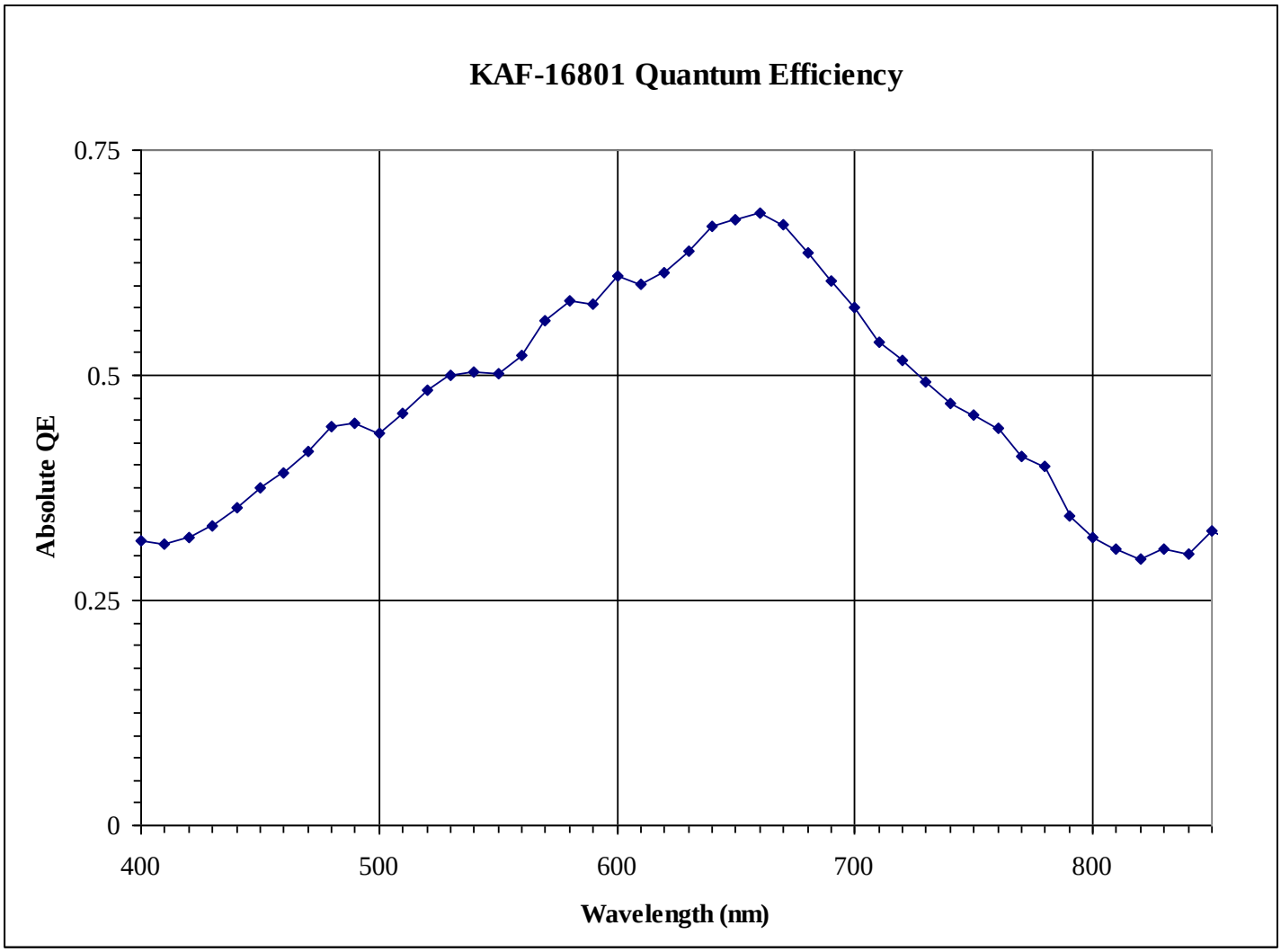


Figure 4: Typical Spectral Response

Dark Current Non Uniformity

The photoresponse non-uniformity specification and the dark signal non-uniformity specification of the sensor both exclude the region that is [1, 1, 400, 400]. The reason for this exclusion is that when the sensor is running with VDD always on, and the integration times are greater than 100 msec, a non-uniformity will become evident surrounding the first pixel. This non-uniformity is a result of the output amplifier emitting light into the photoactive area (see Figure 8). The elevated dark signal in this region typically ranges from 30 electrons/pixel/sec to 100 electrons/pixel/sec, depending on the part, and is independent of temperature. If VDD is switched to 0 volts at least 10 µsec after the last pixel is read out, and switched back to full value 10 µsec before the first pixel of the next frame, the effect of the amplifier glow will be eliminated (see Figure 9).

Defect Definitions

Operating Conditions

All defect tests performed at T = 25 °C

Specifications

Classification	Point Defects	Cluster Defects	Maximum Cluster Size	Column Defects	Maximum Column Width
C1	≤60	≤8	8	4	1
C2	≤120	≤16	8	10	1
C3	≤240	≤32	15	20	2

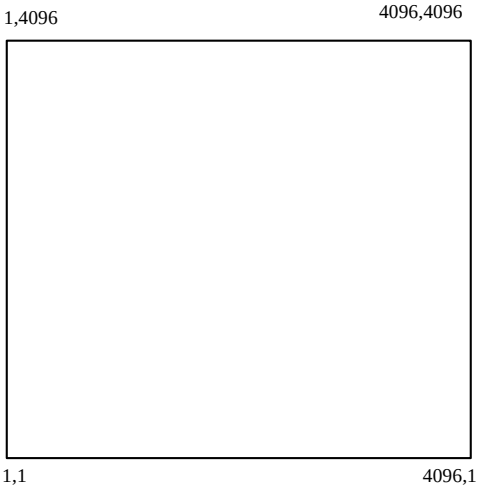


Figure 5: Active Pixel Region

Point Defects

Dark: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation

-- OR --

Bright: A Pixel with dark current > 7,000 e^-/pixel/sec at 25 °C.

Cluster Defect

A grouping of not more than 5 adjacent point defects

Column Defect

A grouping of >5 contiguous point defects along a single column

A column containing a pixel with dark current > 20,000 e^-/pixel/sec, OR A column that does not meet the CTE specification for all exposures less than the specified Max sat. signal level and greater than 2 ke^-

A pixel which loses more than 250 e^- under 2 ke^- illumination

Neighboring Pixels

The surrounding 128 x 128 pixels or ±64 columns/rows

Defect Separation

Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).

Defect Region Exclusion

Defect region excludes the outer two (2) rows and columns at each side/end of the sensor

Operation

Absolute Maximum Ratings

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	Vdiode	0	20	V	1,2
Gate Pin Voltages - Type 1	Vgate1	-16	16	V	1,3
Gate Pin Voltages - Type 2	Vgate2	0	16	V	1,4
Inter-Gate Voltages	Vg-g		16	V	5
Output Bias Current	Iout		-10	mA	6
Output Load Capacitance	Cload		15	pF	6
Storage Temperature	T	-50	70	°C	
Humidity	RH	5	90	%	7

Notes:

1. Referenced to pin Vsub.
2. Includes pins: Vrd, Vdd, Vss, Vout, Vguard.
3. Includes pins: φV1, φV2, φH1, φH2.
4. Includes pins: φR, Vog
5. Voltage difference between overlapping gates. Includes: φV1 to φV2, φH1 to φH2, φV1 to φH2, φH1 to Vog.
6. Avoid shorting output pins to ground or any low impedance source during operation.
7. T = 25 °C. Excessive humidity will degrade MTF.

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	Vrd	11.0	12.0	12.25	V	0.01	
Output Amplifier Return	Vss	1.5	2.0	2.5	V	0.45	
Output Amplifier Supply	Vdd	14.5	15.00	17.0	V	Iout	
Substrate	Vsub	0	0	0	V	0.01	
Output Gate	Vog	4.5	5.0	5.2	V	0.01	
Guard Ring	Vlg	9.0	10.0	12.0	V	0.01	
Video Output Current	Iout	-3.5	-5.0	-10.0	mA		1

Notes:
1. An output load sink must be applied to Vout to activate output amplifier – see Figure 2.

AC Operating Conditions

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance
Vertical CCD Clock - Phase 1	φV1	Low	-9.0	-8.5	-8.3	V	250 nf (all φV1 pins)
Vertical CCD Clock - Phase 1	φV1	High	φV1 low + 10.5	2.0	φV1 low + 10.5	V	250 nf (all φV1 pins)
Vertical CCD Clock - Phase 2	φV2	Low	-9.0	-8.5	-8.3	V	250 nf (all φV2 pins)
Vertical CCD Clock - Phase 2	φV2	High	φV2 low + 10.5	2.0	φV2 low + 10.5	V	250 nf (all φV2 pins)
Horizontal CCD Clock - Phase 1	φH1	Low	-2.5	-2.5	-1.8	V	500 pF
Horizontal CCD Clock - Phase 1	φH1	High	φH1 low + 10.5	2.0	φH1 low + 10.5	V	500 pF
Horizontal CCD Clock - Phase 2	φH2	Low	-2.5	-2.5	-1.8	V	300 pF
Horizontal CCD Clock - Phase 2	φH2	High	φH2 low + 10.5	2.0	φH2 low + 10.5	V	300 pF
Reset Clock	φR	Low	3.0	5.0	5.5	V	10 pF
Reset Clock	φR	High	9.5	10.0	10.5	V	10 pF

Notes:
1. All pins draw less than 10 µA DC current.
2. Capacitance include gate to VSUB and gate to gate (φV1-φV2, φH1-φH2).

Timing

Requirements and Characteristics

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
φH1, φH2 Clock Frequency	f_H		8	15	MHz	1, 2, 3
φV1, φV2 Clock Frequency	F_V		25	25	kHz	1, 2, 3
Pixel Period (I count)	t_e	67	125		ns	
φH1, φH2 Setup Time	$t_{\phi HS}$	0.5	1		µs	
φV1, φV2 Clock Pulse Width	$t_{\phi V}$	40	40		µs	2
φV1, φV2 Clock Pulse Overlap	t_{ovrlp}	20	20			
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	1398	2390		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	338.7	580		µs	7

Notes:

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
4. φR should be clocked continuously.
5. $t_{readout} = (4128\ t_{line})$
6. Integration time is user specified. Longer integration times will degrade noise performance.
7. $t_{line} = (2* t_{\phi V}) - t_{ovrlp} + t_{\phi HS} + (4145 * t_e) + t_e$.

Frame Timing

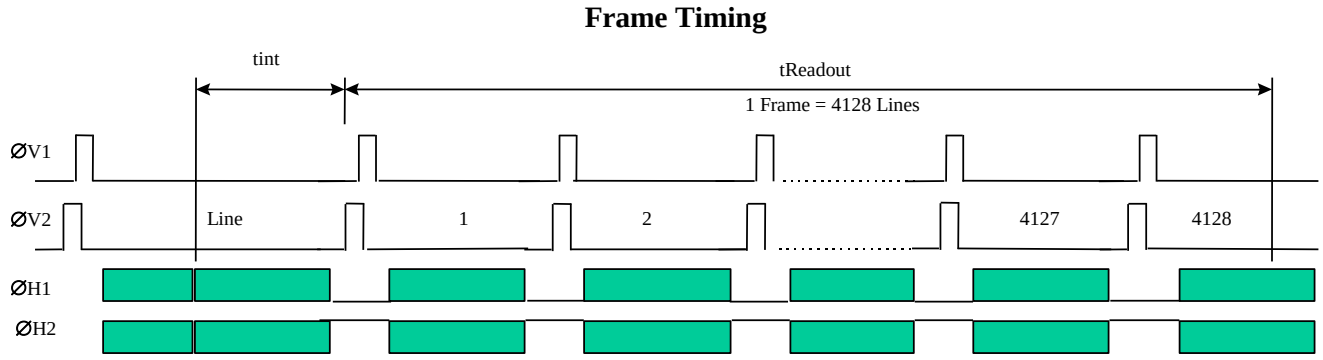


Figure 6: Frame Timing

Line Timing (Each Output)

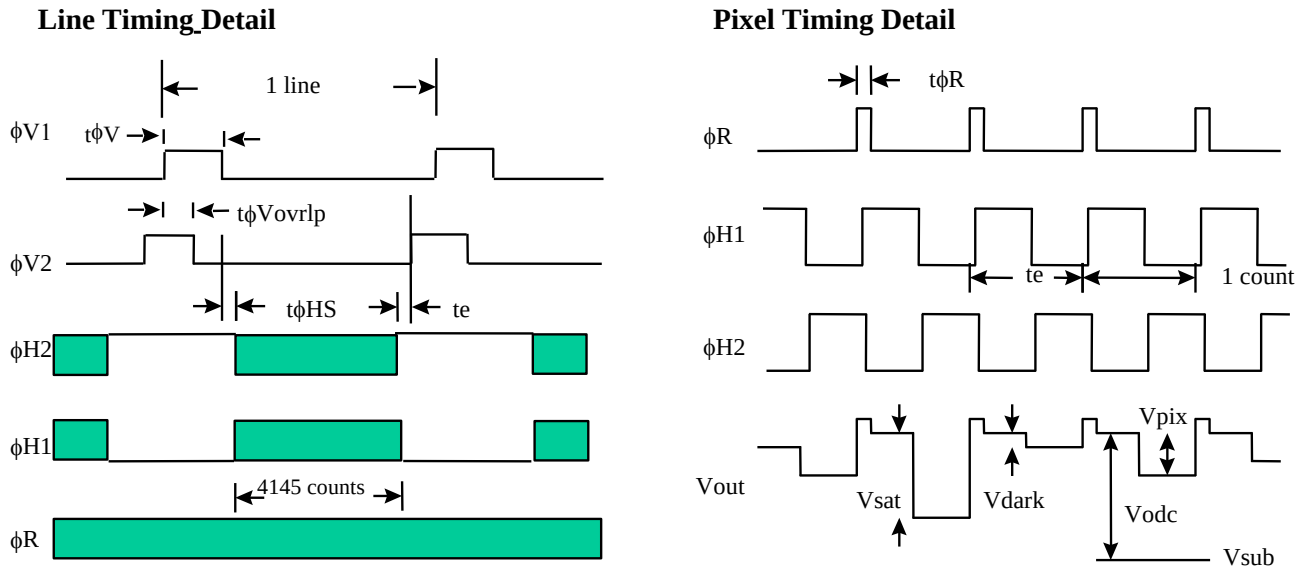
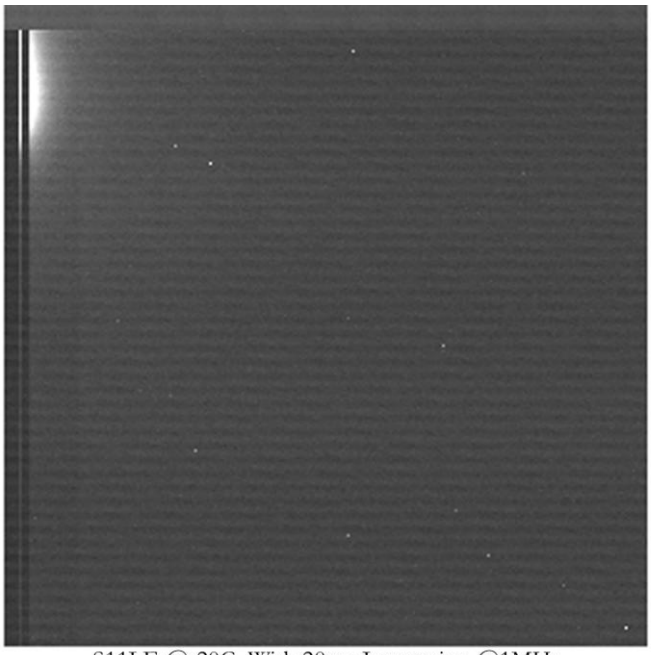
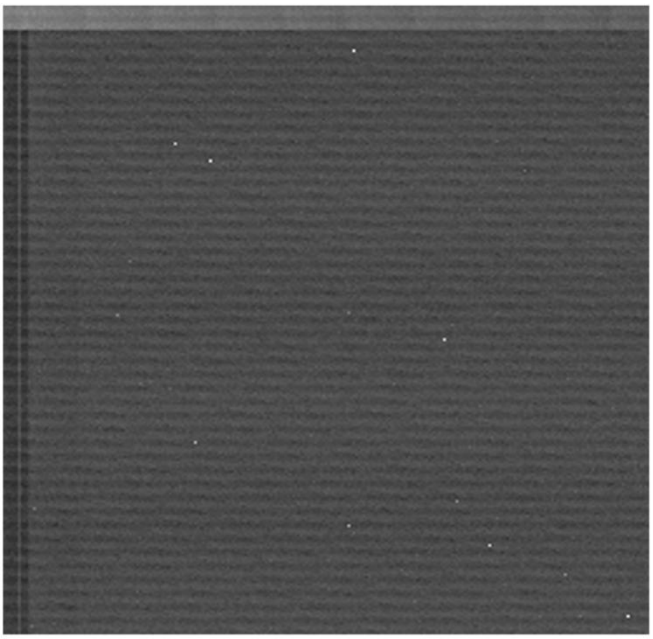


Figure 7: Line Timing



S11LE @-20C With 20sec Integration @1MHz
VDD Always On (+15)

Figure 8: Amplifier Glow



S11LE @-20C With 20sec Integration @1MHz
VDD Off During Integration

Figure 9: Amplifier Glow

Notes:

1. Amplifier glow is suppressed by switching VDD to 0 volts during integration.

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	100	°C	1
Operating Temperature	T_{OP}	-60	60	°C	

Notes:
1. Storage toward the maximum temperature will accelerate microlens degradation.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Information

COMPLETED ASSEMBLY

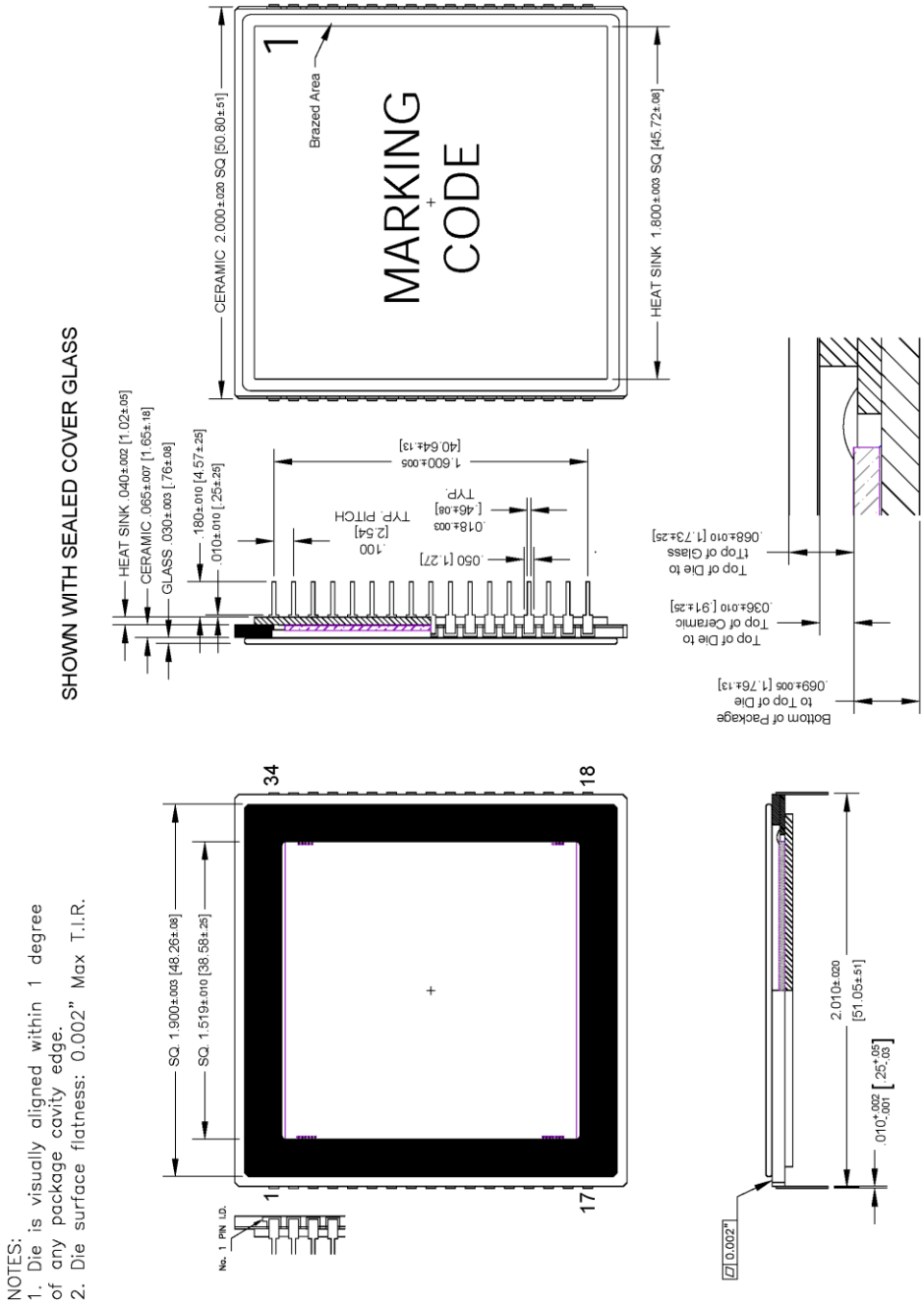


Figure 10: Completed Assembly (1 of 2)

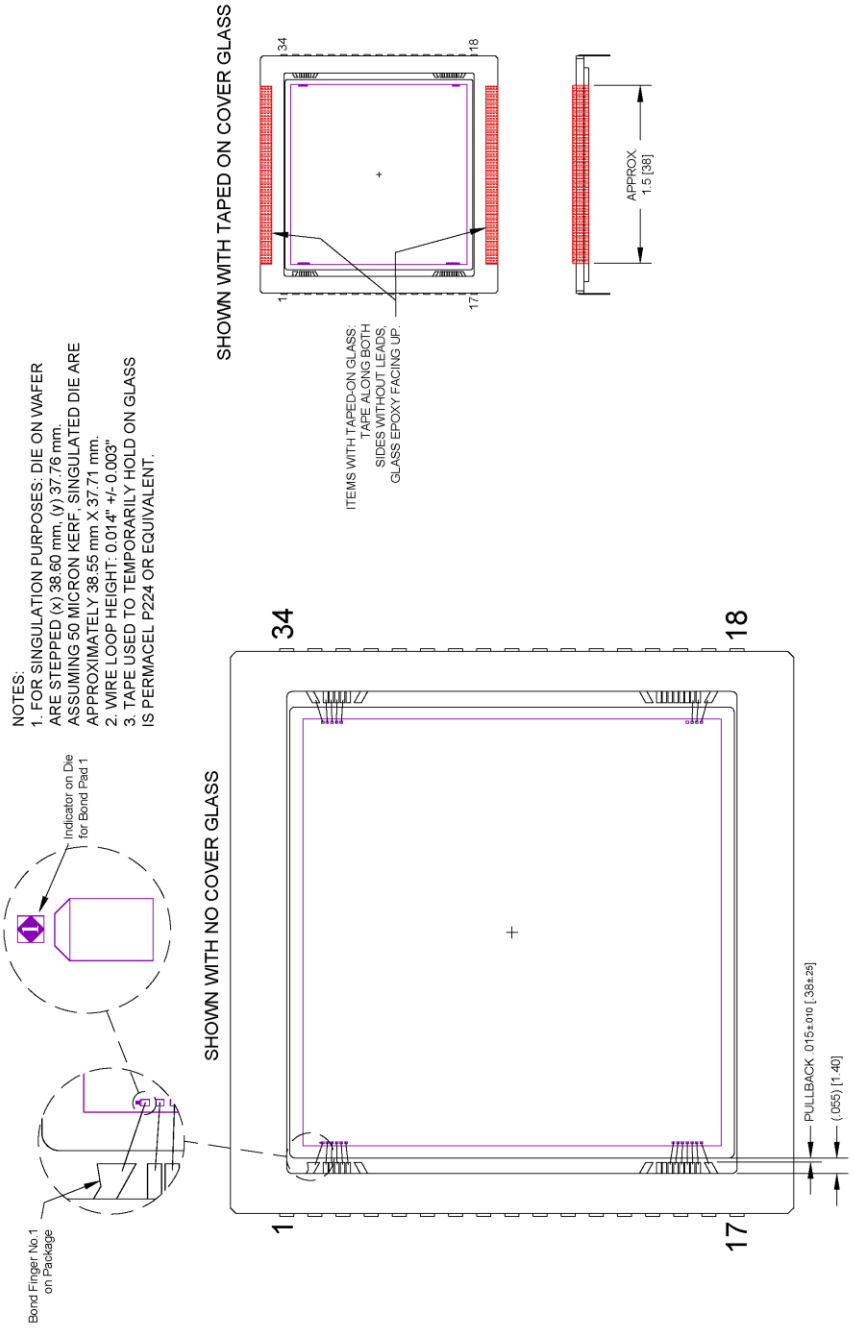


Figure 11: Completed Assembly (2 of 2)

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from Truesense Imaging upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

Truesense Imaging reserves the right to change any information contained herein without notice. All information furnished by Truesense Imaging is believed to be accurate.

Life Support Applications Policy

Truesense Imaging image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of Truesense Imaging, Inc.

Revision Changes

MTD/PS-1128

Revision Number	Description of Changes
1.0	• Initial Release.
2.0	• Removed S11LE parts numbers and references.
2.1	• Updated φV1, φV2 Clock Frequency units and wavelength band figures.

PS-0032

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections