

## Linear X-Ray Photodiode Detector Array with Signal Amplification

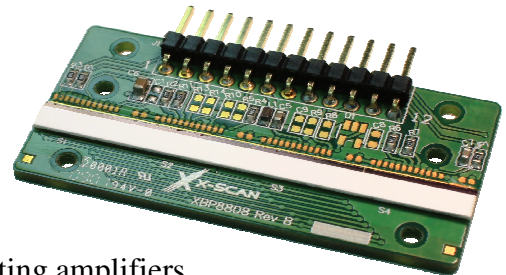
# XB8816R Series

An X-Scan Imaging XB8816R linear detector array is constructed of CMOS silicon photodiode array detector chips mounted on a single printed-circuit board. The imaging circuit of each detector chip consists of a contiguous linear array of photodiodes, a timing generator, digital scanning shift register, an array of charge integrating amplifiers, sample-and-hold circuits, and signal amplification chain. Each detector array generates an End-Of-Scan (EOS) pulse that can be used to initiate the scanning of the next detector array. Thus, a longer, continuous detector array can be formed from a daisy chain of smaller detector arrays.

For x-ray scanning applications, a scintillator material tailored to the user's application is attached to the surface of the detector array to convert x-ray photons into visible light for detection by the photodiode array. The XB8816R photodiode array is uniquely designed and processed to reduce radiation damage from the x-ray flux. The signal processing circuits are positioned 2 mm away from the photodiode array. These circuits are shielded from direct x-ray radiation using an external heavy-metal shield. The precision alignment of the metal shield with respect to the signal processing circuits is performed at the factory using a special molded housing and chip-on-board (COB) technology.

### Key Features

- Large element pitch resolution of 1.6 mm
- Different array lengths available:
  - 2.0 inches (32 pixels)
  - 4.0 inches (64 pixels)
  - etc.
- 5-V power supply operation
- Simultaneous integration by using an array of charge integrating amplifiers
- Sequential readout with a digital scanning shift register (Data rate: 1 MHz max.)
- Integrated CDS circuits allow low noise and wide dynamic range up to > 4000
- User-specified scintillator material GOS:Tb, CsI:Tl, CdWO<sub>4</sub>, etc.
- Extended radiation hardness lifetimes



### Applications

- Linear x-ray imaging for industrial and food inspection
- Linear x-ray imaging for homeland security and cargo screening

## ■ Mechanical specifications

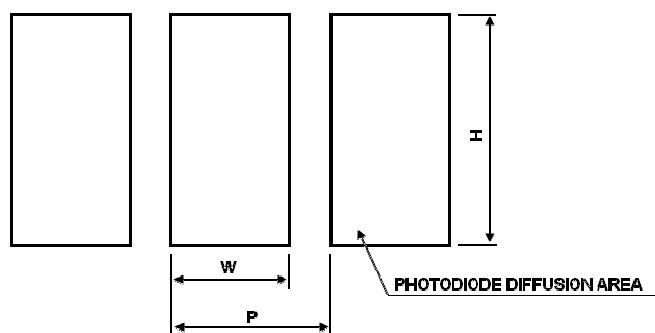
Parameter	Symbol <sup>i</sup>	XB8816R-2.0 <sup>ii</sup>	XB8816R-4.0 <sup>iii</sup>	Unit
Element pitch	P	1.6	1.6	mm
Element diffusion width	W	1.565	1.565	mm
Element height	H	2.4	2.4	mm
Number of elements	–	32	64	–
Active area length	–	51.2	102.4	mm

<sup>i</sup> Refer to enlarged view of active area figure.

<sup>ii</sup> 2-inch long detector is specified here. Other lengths (at multiples of 0.5 inches) are available upon request.

<sup>iii</sup> 4-inch long detector is specified here. Other lengths (at multiples of 0.5 inches) are available upon request.

## ■ Enlarged view of active area



## ■ Absolute maximum ratings



*Electronic device sensitive to electrostatic discharge and x-ray radiation.* Although this device features ESD protection circuitry, permanent damage ranging from subtle performance degradation to complete device failure may occur on devices subjected to high-energy electrostatic discharges. Furthermore, although this device features radiation shielding for protection against anticipated x-ray radiation, permanent damage ranging from subtle performance degradation to complete device failure may occur on devices subjected to unanticipated x-ray radiation (e.g. off-axis or extremely high energy radiation). Therefore, proper precautions against ESD and x-ray radiation must be taken during handling and storage of this device.

Parameter	Symbol	Min	Max	Unit
Supply voltage	VDD	–0.3	+6	V
Reference voltage	VREF	–0.3	VDD + 0.3	V
Digital input voltages		–0.3	VDD + 0.3	V
Operating temperature <sup>iv</sup>	T <sub>opr</sub>	–5	+60	°C
Storage temperature	T <sub>stg</sub>	–10	+70	°C

<sup>iv</sup> Humidity must be controlled to prevent the occurrence of condensation.

## ■ Recommended terminal voltage

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	4.75	5	5.25	V
Reference voltage	VREF	–	4.50	–	V

## ■ Electrical characteristics [Ta = 21°C, VDD = 5 V]

Parameter	Symbol	Min.	Typ.	Max.	Unit	
<b>Digital</b>						
Clock pulse frequency <sup>v</sup>	f(CLK)	40	–	4000	KHz	
Digital input voltage <sup>vi</sup>	High level	Vih	VDD–1.00	VDD	V	
	Low level	Vil	0	0	0.4	V
Digital input capacitance	Ci	–	40	–	pF	
Digital input leakage current	Ii	–10	+10	–	μA	
Digital output voltage <sup>vii</sup>	High level	Voh	VDD–0.75	VDD	V	
	Low level	Vol	0	0	0.4	V
Digital output load capacitance	Co	–	–	50	pF	
<b>Analog</b>						
Reference voltage input impedance <sup>viii</sup>	Rref	–	5	–	KΩ	
Charge amplifier feedback capacitance <sup>ix</sup> (PG2:PG1)	0:0	Cf00	–	16	–	pF
	0:1	Cf01	–	8	–	pF
	1:0	Cf10	–	4	–	pF
	1:1	Cf11	–	2	–	pF
Video output impedance	Zv	–	1	–	KΩ	
Video output load capacitance	Cv	–	–	100	pF	
<b>Power</b>						
Power consumption	P	–	200	–	mW	

<sup>v</sup> Video rate is 1/4 of clock pulse frequency f (CLK).

<sup>vi</sup> Digital inputs include CLK, RESET, EXTSP, PG2, and PG1.

<sup>vii</sup> Digital outputs include Trig and EOS (see pin connections).

<sup>viii</sup> Reference voltage input impedance is dependent on length of detector. For a 2-inch detector (XB8816R-2.0), the input impedance is 5 KΩ.

<sup>ix</sup> The sensitivity selection pins (see PG2:PG1 pin connections) control the sensitivity of the detector by selecting the pixel charge amplifier feedback capacitance from Cf00 to Cf11. At Cf00, the detector has lowest sensitivity. At Cf11, the detector has highest sensitivity.

## ■ Radio-opto-electrical characteristics [Ta = 21°C, VDD = 5 V]

Parameter	Symbol	XB8816R (1.6mm)			Unit
		Min.	Typ.	Max.	
Output offset voltage <sup>x</sup>	Vos	–	VREF	–	V
Dark offset voltage <sup>xi</sup>	Vd	–40	–	40	mV
X-ray sensitivity <sup>xii</sup> (PG2:PG1)	S	1:1	12000	–	V/R
		1:0	6000	–	
		0:1	3000	–	
		0:0	1500	–	
Photo response non-uniformity <sup>xiii</sup>	PRNU	–10	–	10	%
Noise <sup>xiv</sup>	N	PG2:PG1 = 0:0	0.75	–	mVrms
		PG2:PG1 = 1:1	2.00	–	
Saturation output voltage	Vsat	3.0	–	–	V

<sup>x</sup> Video output is negative-going output with respect to the output offset voltage.

<sup>xi</sup> Difference between output signal under dark conditions and Vref with an integration time of 1 ms.

<sup>xii</sup> Sensitivity is dependent on x-ray source. Other scintillations with different sensitivity are available.

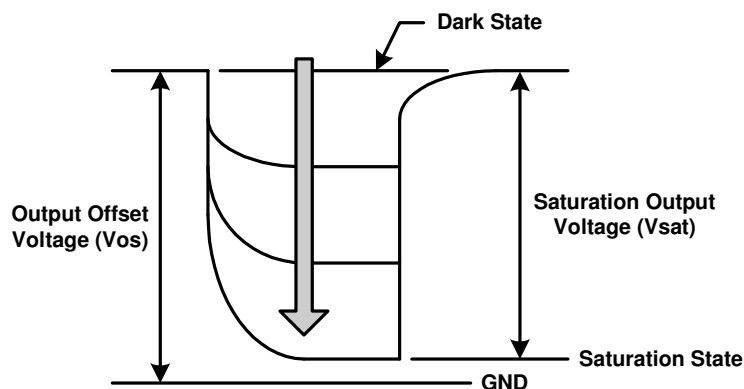
<sup>xiii</sup> Measured without scintillation. When the photodiode array is exposed to uniform light which is 50% of the saturation exposure, the Photo Response Non Uniformity (PRNU) is defined as follows:

$$PRNU = \Delta X \div X \times 100\%$$

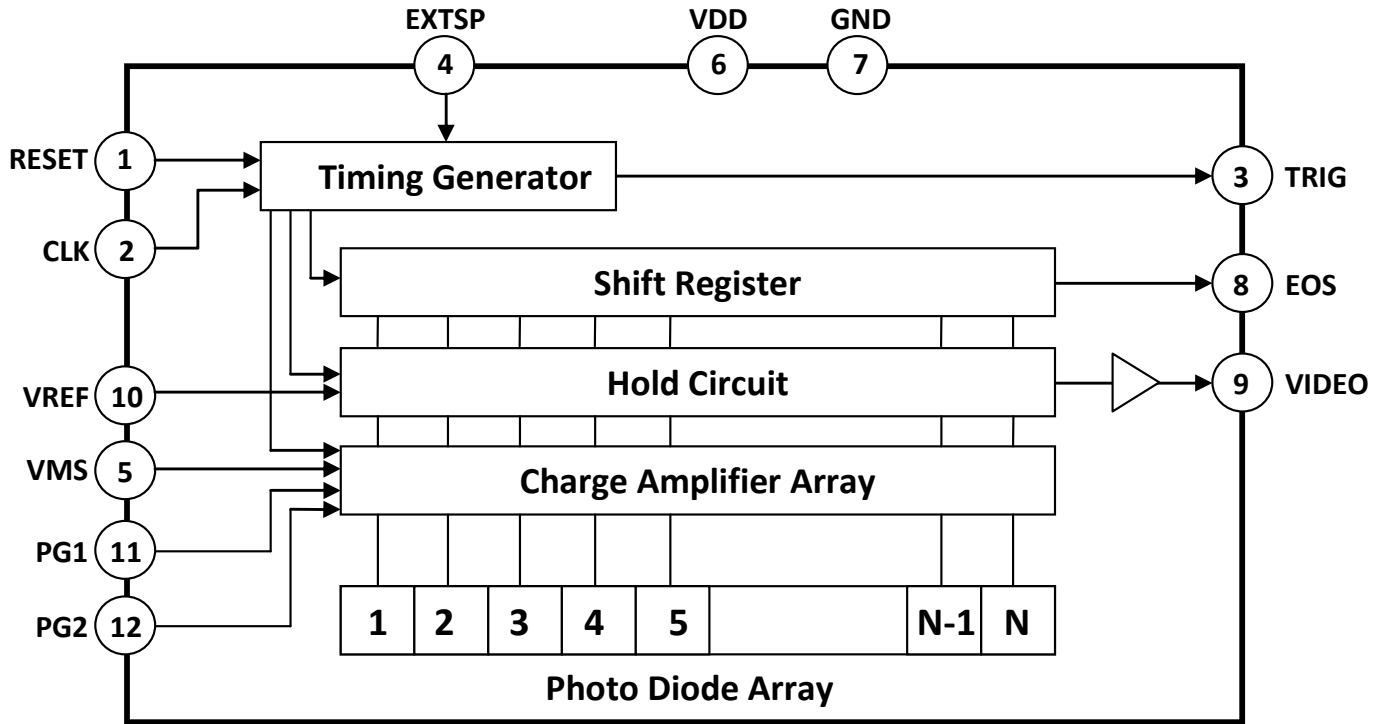
where X is the average output of all elements and ΔX is the difference between the maximum and minimum outputs.

<sup>xiv</sup> Measured with a video data rate of 750 KHz and an integration time of 1 ms in dark state.

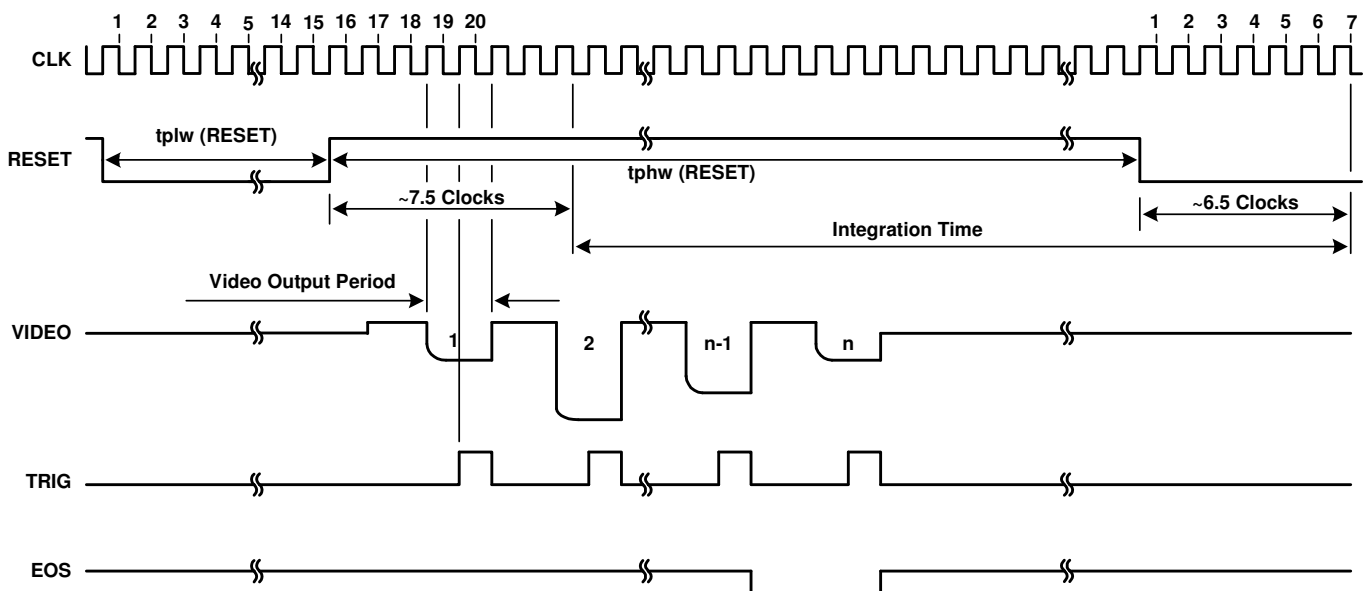
## ■ Output waveform of one element

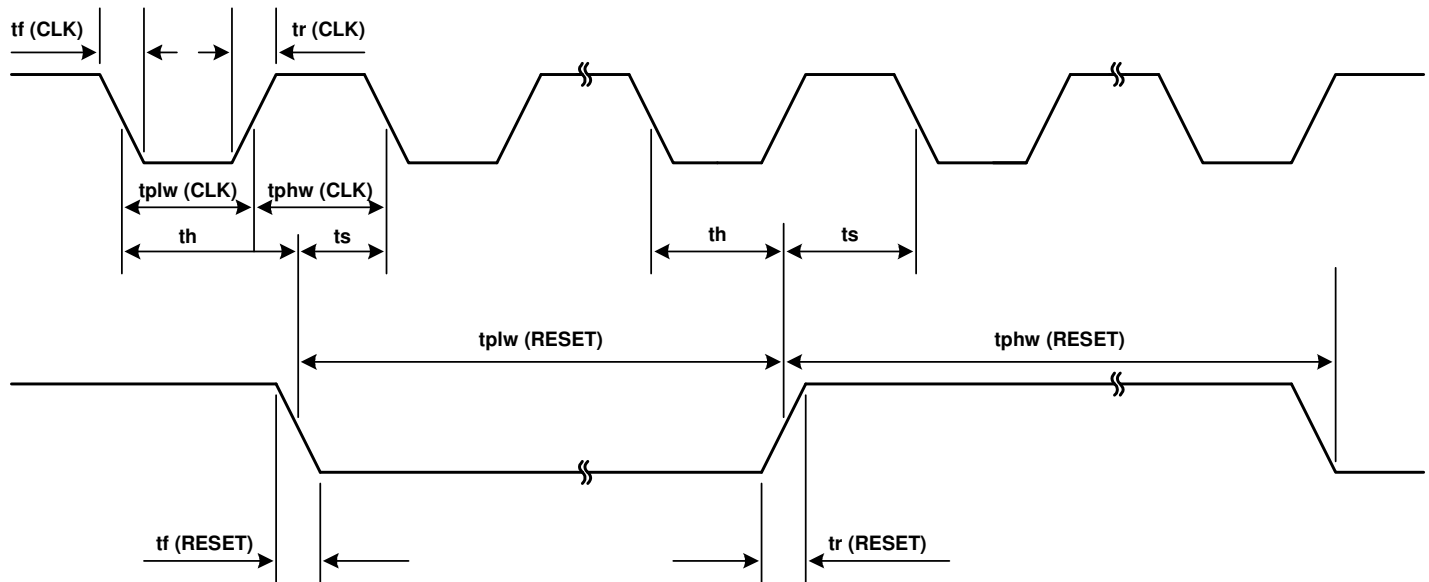


## ■ Block diagram



## ■ Timing chart<sup>xv</sup>





Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse low/high width	tplw (CLK), tphw (CLK)	100	–	–	ns
Clock pulse rise/fall times	tr (CLK), tf (CLK)	0	20	30	ns
Reset pulse low width <sup>xvi</sup>	tplw (RESET)	12 / f(CLK)	16 / f(CLK)	–	ms
Reset pulse high width <sup>xvii</sup>	tphw (RESET)	20	–	–	μs
Reset pulse rise/fall times	tr (RESET), tf (RESET)	0	20	30	ns
Reset pulse setup time <sup>xviii</sup>	ts	40	–	–	ns
Reset pulse hold time	th	40	–	–	ns

<sup>xv</sup> The falling of Video just before the 19<sup>th</sup> falling edge of CLK after transition of RESET from High to Low corresponds to the first pixel. The video output for the first pixel should be read around the 20<sup>th</sup> falling edge and before the subsequent rising CLK edge while Trig is high. After the first pixel, a pixel output appears on Video at every 4th clock cycle.

Care should be taken to prevent the rising edge of the RESET during the video output. Improper positioning of the RESET edges can lead to interference with the read-out.

The falling edge of the RESET should follow the last pixel of the previous line's read-out. Thus, one cycle of RESET pulses cannot be set shorter than the time equal to  $(17 + 4 \times N)$  clock cycles, where N is the number of pixels.

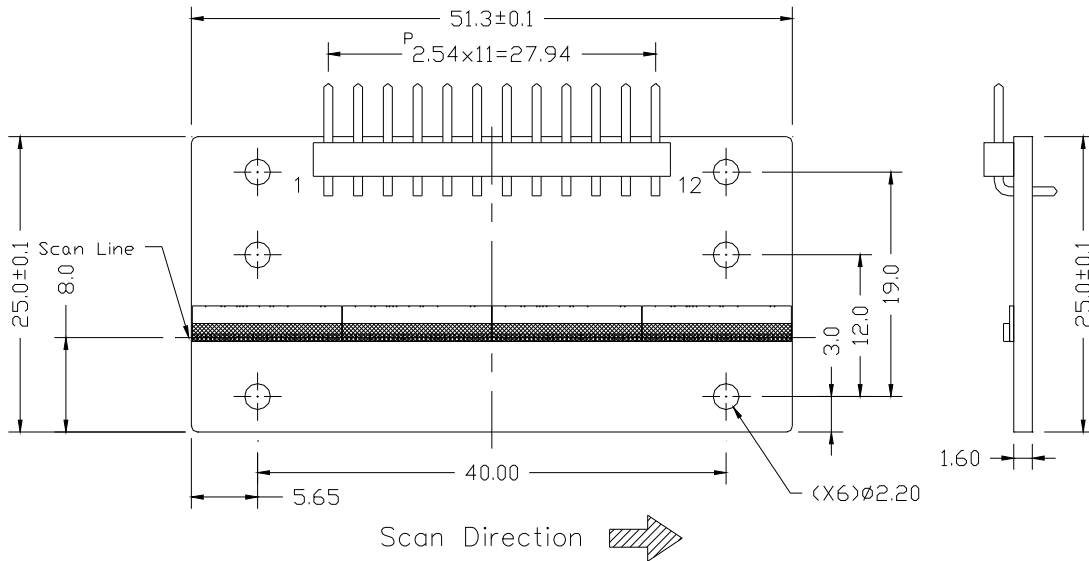
EOS of each detector chip appears during the output of the last pixel.

<sup>xvi</sup> RESET must stay Low [tplw(RESET)] for at least twelve clock cycles.

<sup>xvii</sup> The falling edge of RESET pulse determines the end of the integration time and the start of signal read-out, while the rising edge of the RESET pulse determines the start of the integration time. As a result, the signal-charge integration time can be controlled externally with the width of the RESET pulse [tphw(RESET)]. However, the charge integration does not start at the rise of a RESET pulse but starts at the 8<sup>th</sup> falling edge of clock after the rise of the RESET pulse and ends at the 7<sup>th</sup> falling edge of clock after the fall of the RESET pulse.

<sup>xviii</sup> The rising and falling edges of RESET must observe the setup and hold time requirements around the falling edges of CLK.

## ■ Mechanical drawings<sup>xix</sup>



<sup>xix</sup> Unit: Dimensions are in millimeters (mm).

Board: FR4 epoxy resin bonded glass fabric.

Connector: BISON Advanced Technology Corp., Ltd. ([www.bison-protech.com](http://www.bison-protech.com)), P101-RGP-060/030-12 or similar.

## ■ Pin connections

Pin No.	Symbol	Name	Description
1	RESET	Reset Pulse	Negative-going pulse input
2	CLK	Clock Pulse	Pulse input
3	TRIG	Trigger Pulse	Positive-going pulse output
4	EXTSP	External Start Pulse	Pulse/voltage input
5	VMS	Master/Slave Selection	See sensitivity selection table
6	VDD	Supply Voltage	5-V supply voltage
7	GND	Ground	Common ground voltage
8	EOS	End of Scan	Negative-going pulse output
9	VIDEO	Video Output	Negative-going output with respect to VREF
10	VREF	Reference Voltage	Voltage input
11	PG1	Sensitivity Selection	See sensitivity selection table
12	PG2	Sensitivity Selection	See sensitivity selection table

## ■ Sensitivity Selection Table

Sensitivity Mode	PG2	PG1	Relative Sensitivity
1	GND	GND	1/8
2	GND	VDD	1/4
3	VDD	GND	1/2
4	VDD	VDD	1

## ■ Master/slave selection with start pulse EXTSP settings (VMS=GND)

For most applications, multiple detectors are read out in parallel. To ensure parallel read out, set the EXTSP inputs of all detectors to LOW (A in the table below).

In applications where two or more linearly connected detectors are read out sequentially (in series), set the first detector's EXTSP to LOW while connecting the EXTSP input of each subsequent detector to the EOS output of each respective preceding detector (B in the table below). The CLK and RESET pulses should be shared among all detectors and the Video output terminals of all detectors are connected together. The maximum number of detectors that can be daisy-chained together is limited by the maximum Video output capacitance requirement.

	Operation Mode	EXTSP
A	Master configuration: Parallel readout: all detectors Serial readout: 1 <sup>st</sup> detector only	LOW
B	Slave configuration: Serial readout: 2 <sup>nd</sup> and later detectors	Preceding detector's EOS should be input

## ■ Master/slave selection voltage VMS and external start pulse EXTSP settings

For most applications, multiple detectors are read out in parallel. To ensure parallel read out, set the VMS input of all detectors to VDD (A in the table below).

In applications where two or more linearly connected detectors are read out sequentially (in series), set the VMS input of the first detector to VDD and the VMS input of each subsequent (second and later) detector to GND while connecting the EXTSP input of each subsequent detector to the EOS output of each respective preceding detector (B in the table below). The CLK and RESET pulses should be shared among all detectors and the Video output terminals of all detectors are connected together. The maximum number of detectors that can be daisy-chained together is limited by the maximum Video output capacitance requirement.

	Operation Mode	VMS	EXTSP
A	Master configuration: Parallel readout: all detectors Serial readout: 1 <sup>st</sup> detector only	VDD	Don't care
B	Slave configuration: Serial readout: 2 <sup>nd</sup> and later detectors	GND	Preceding detector's EOS should be input



## ■ Readout circuit

In order to minimize noise and to maximize performance, an operational amplifier should be placed close to the detector to amplify the Video signal.

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107 Bonaventura Dr., San Jose, CA 95134, U.S.A.

Tel: +1 408 432 9888

Fax: +1 408 432 9889

[www.x-scanimaging.com](http://www.x-scanimaging.com)