# Development of 4-Sides Buttable CdTe-ASIC Hybrid Module for X-ray Flat Panel Detector

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***Abstract*—A 4-sides buttable CdTe-ASIC hybrid module suitable for use in an X-ray flat panel detector (FPD) has been developed by applying through silicon via (TSV) technology to the readout ASIC. The ASIC has 128 $\times$ 256 channels of charge integration type readout circuitry and an area of 12.9 mm $\times$ 25.7 mm. The CdTe sensor of 1 mm thickness, having the same area and pixel of 100 $\mu$m pitch, was fabricated from the Cl-doped CdTe single crystal grown by traveling heater method (THM). Then the CdTe pixel sensor was hybridized with the ASIC using the bump-bonding technology. The basic performance of this 4-sides buttable module was evaluated by taking X-ray images, and it was compared with that of a commercially available indirect type CsI(Tl) FPD. A prototype CdTe FPD was made by assembling 9 pieces of the 4-sides buttable modules into 3 $\times$ 3 arrays in which the neighboring modules were mounted on the interface board. The FPD covers an active area of 77 mm $\times$ 39 mm. The results showed the great potential of this 4-sides buttable module for the new real time X-ray FPD with high spatial resolution.**

***Index Terms*—CdTe, four-sides buttable, through-silicon-via, X-ray imaging.**

## I. Introduction

CADMIUM TELLURIDE (CdTe) is a promising material for X-ray imaging detectors in the field of the medical, dental and nondestructive testing applications because of the high detective quantum efficiency and high energy resolution for X-ray. Various types of CdTe-ASIC hybrid modules had been already developed for X-ray imaging [1], [2]. Fig. 1(a) shows a schematic view of the structure for conventional CdTe-ASIC hybrid module. However, as long as they use the ASIC with conventional structure where the I/O pads are arranged along one edge of the ASIC to be wire-bonded to an interface board, the I/O pads area of the ASIC causes an inevitable dead space for plural hybrid modules to be assembled adjoining each other. After all, this structure of the so-called 3-sides buttable CdTe-ASIC hybrid modules has restricted the arrangement of the modules for a two-dimensional X-ray imager.

By eliminating the wire-bonding and the dead space from the conventional structure, an active area of the CdTe sensor can be extended up to the edge of the ASIC shown in Fig. 1(b). The so-called 4-sides buttable structure is realized by using these modules which can be assembled in all four directions. In this work, we describe the development of the 4-sides buttable CdTe-ASIC hybrid module for a Flat Panel Detector (FPD).

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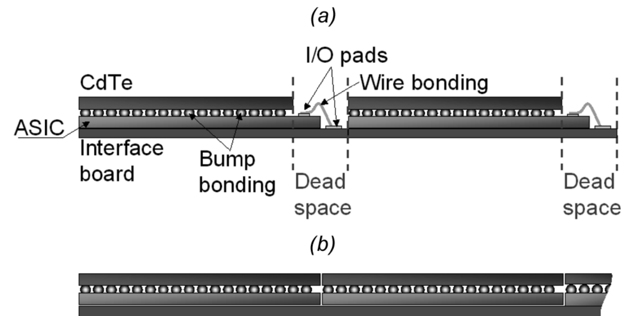


Fig. 1. Structure of (a) the conventional CdTe-ASIC hybrid module and (b) the 4-sides buttable CdTe-ASIC hybrid module.

## II. Material and Method

### A. Through Silicon Via (TSV)

Through Silicon Via (TSV) technology, which has been recently developed for the advanced Silicon devices having three-dimensional stacking structure, was applied to the readout pixel ASIC to eliminate the wire-bonding and the dead space from 3-sides buttable module. Fig. 2 shows (a) a schematic view of TSV near the edge of the ASIC and (b) a cross sectional image of TSV near the front-side I/O pad. Via holes were etched from the back-side of ASIC to reach the front-side I/O pad. The diameter and the depth of via hole are 80 $\mu$m and 250 $\mu$m, respectively. The oxide insulation layer and the conductive layer were formed on the sidewall of via and they were extended to be connected to the new back-side I/O pads of the ASIC. The surface of the ASIC was protected by the passivation layer. Total number of I/O pads and via holes is 26 which are formed along one edge of the ASIC chip and they are divided into analog and digital lines which have the function of GND, analog output, ASIC configuration, power supply, clock, and tuning. The fabrication of TSV was carried out in a Silicon MEMS foundry.

### B. Hybridization

The CdTe sensor was fabricated from the Cl-doped CdTe single crystal grown by Traveling Heater Method (THM) [3], [4]. CdTe single crystal wafers of 1 mm thickness were sliced from CdTe ingot with (111) orientation and polished mechanically and chemically. The Schottky contact was formed on CdTe wafers using indium (In) as a common electrode and platinum (Pt) as pixel electrodes. The thickness of the indium layer is

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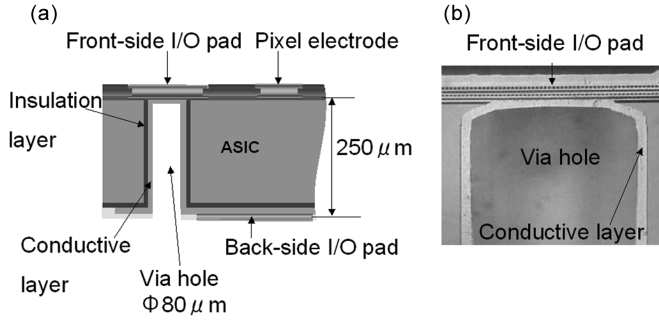


Fig. 2. (a) Schematic view of TSV near the edge of the ASIC and (b) a cross sectional image of TSV near the front-side I/O pad.

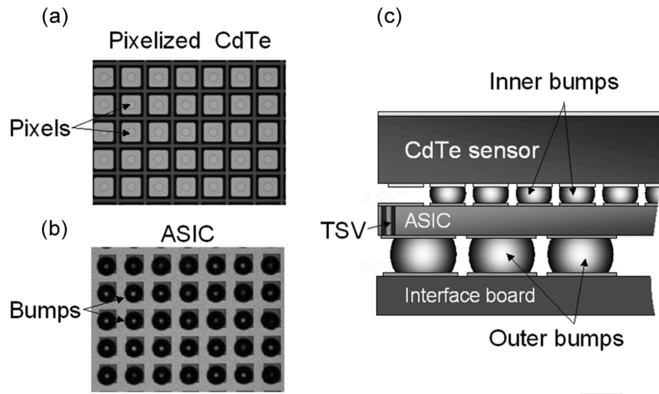


Fig. 3. Photographs of the surface of (a) the pixelized CdTe sensor and (b) the ASIC. (c) A schematic view of the 4-sides buttable hybrid module.

300 nm. Fig. 3(a) shows a photograph of the pixel electrode of the CdTe sensor. Pixel size is 70 $\mu\text{m}$ square and pixel pitch is 100 $\mu\text{m}$. The diameter of contact hole for bump bonding is 30 $\mu\text{m}$. The CdTe sensor has $128 \times 256 (= 32,768)$ pixels. A 15-$\mu\text{m}$-wide guard ring is formed surrounding most outer pixels, which is well known to block the leakage current injection from the edge of the CdTe sensor to pixel electrodes [5]. The distance between the most outer pixel and the guard ring electrode is 15 $\mu\text{m}$, and the distance from the edge of the CdTe sensor to the guard ring is 25 $\mu\text{m}$.

The ASIC was designed for integration and read out of charge pulses from a CdTe sensor working in hole collection mode. The ASIC was fabricated with AMIS 0.35- $\mu\text{m}$ CMOS technology. The ASIC has $128 \times 256 (= 32,768)$ pixels with a pitch of 100 $\mu\text{m}$. Each pixel contains a bump bonding pad, an input transistor, an integration capacitor, a sampling capacitor, a buffer amplifier and switches to control the sampling, reset and readout of the integrated charge. The total power consumption is less than 15 mW. The frame rate can be set up to 50 fps for a fast moving object. Fig. 3(b) shows a photograph of the pixel electrode of the ASIC. Bumps were formed on pixel electrodes of the ASIC in wafer level process. The soldering bumps with the low melting point were used to avoid the damage for the CdTe sensor. The CdTe sensor was hybridized with the ASIC using the flip-chip-bonding technology shown in Fig. 3(c). These hybrid bare modules were mounted on the interface board and heated during the re-flow process. Back side I/O pads of the ASIC were connected to the interface board by outer bumps.

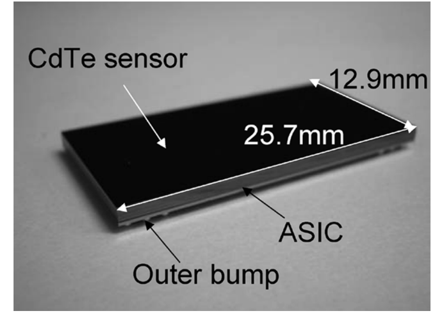


Fig. 4. Photograph of the 4-sides buttable hybrid module.

TABLE I
THE SPECIFICATIONS OF THE 4-SIDES BUTTABLE HYBRID MODULE

| Specifications | |
|---|---|
| CdTe thickness | 1 mm |
| Pixel pitch | 100 μm |
| Total number of pixels | 32,768 pixels |
| Active area | 12.9 mm x 25.7 mm |
| Operation type | Charge integration |
| Maximum frame rate | 50 fps |

Outer bumps with the diameter of 750 $\mu\text{m}$, which are larger than inner bumps with the diameter of 60 $\mu\text{m}$, were used.

The photograph and the specification of the 4-sides buttable hybrid bare module are shown in Fig. 4 and Table I, respectively.

## III. Results and Discusstion

### A. Spatial Resolution

The spatial resolution characteristic was evaluated by taking an X-ray image of a resolution chart pattern. A micro focus X-ray source (HAMAMATSU L9181S) was used for the measurement. The X-ray source has a focal spot size of 40 $\mu\text{m}$. The distance between the X-ray source and the surface of the CdTe hybrid module was 60 cm. The measured dose rate without the filtration was approximately 800 mR/min at tube voltage of 80 kV and tube current of 100 $\mu$A. A commercially available indirect X-ray conversion type CsI(Tl) FPD with the same pixel pitch was used for the comparison [6]. The CsI(Tl) FPD utilize a 200- $\mu\text{m}$-thick CsI (Tl) scintillator plate with a needle structure. Fig. 5 shows the X-ray images taken by the CsI(Tl) and the CdTe at 80 kV. For CsI(Tl), it was difficult to discriminate line pairs at 5 lp/mm which corresponded to the theoretical Nyquist frequency. On the other hand, for the CdTe it was clearly visible. The CdTe shows excellent spatial resolution characteristics.

The pre-sampling Modulation Transfer Function (MTF) was measured by the edge method which was the standardized method to evaluate the spatial resolution characteristics for medical digital X-ray imaging devices [7]. A tungsten plate

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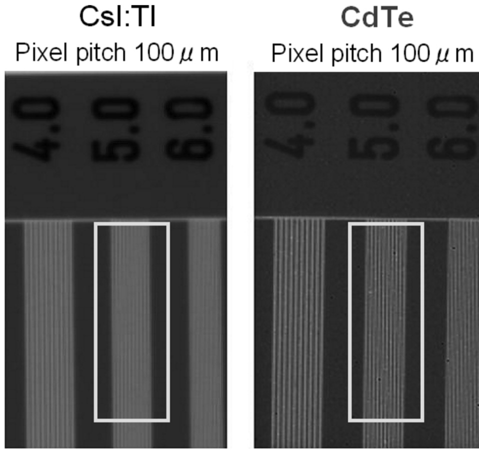


Fig. 5. Comparison of X-ray images of a resolution chart pattern taken by the CsI(Tl) FPD and the CdTe module at 80 kV.

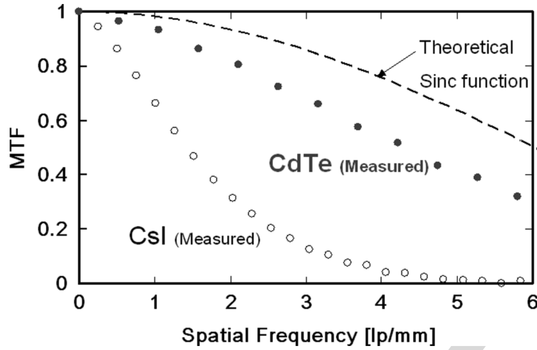


Fig. 6. Comparison of the pre-sampling MTF for CsI(Tl) FPD and CdTe module as a function of spatial frequency. Open and filled circles show the MTF for CsI FPD and the CdTe module, respectively. The theoretical sinc function curve was also plotted (dashed line).

with 1 mm thickness was placed in front of the hybrid module surface with the distance of 5 mm. The edge of the plate was aligned to the center axis of the X-ray beam and tilted by an angle less than 3 ° relative to the axis of the pixel rows. An X-ray image of the edge of the plate taken at 80 kV was analyzed. The MTF was calculated from a Fourier transform of the line spread function (LSF) of the edge at three different positions. Fig. 6 shows a comparison of the MTF curves for the CsI(Tl) FPD and the CdTe hybrid module. The horizontal and the vertical axes represent the spatial frequency and the MTF, respectively. Filled and open circles show the MTF curves for the CdTe module and CsI(Tl) FPD, respectively. The MTF value of the CdTe module was found to be significantly higher than that of the CsI(Tl) FPD in all frequency range investigated here. The theoretical sinc function with the pixel pitch of 100 $\mu$m was also plotted in Fig. 6 (dashed line). The MTF curve of the CdTe was lower than the sinc function. This difference could be explained by the inter-pixel signal leakage according to [2].

### *B. Performance of Prototype CdTe FPD*

A prototype CdTe FPD was made by assembling 9 pieces of the 4-sides buttable bare modules on an interface board into

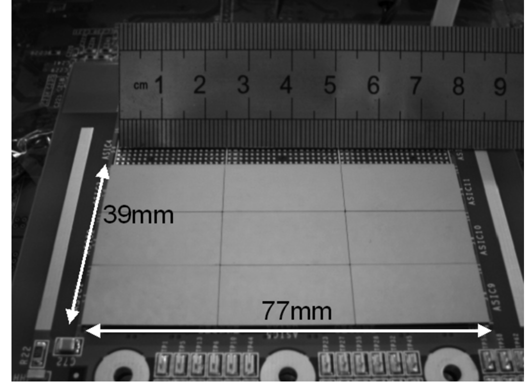


Fig. 7. Photograph of a prototype CdTe FPD by assembling 9 pieces of the 4-sides buttable modules into 3 × 3 arrays.

3 × 3 arrays with the gap of 50 $\mu$m among neighboring hybrids shown in Fig. 7. The dead space corresponding to one-line-width was induced among neighboring hybrids where the center-to-center distance of most outer pixels of neighboring hybrids was 230 $\mu$m. The FPD covers the active area of 39 mm × 77 mm.

The bias voltage of 500 V was applied to the top electrodes of all modules. A periodic bias reset technique was used to suppress the polarization effect [8]. The polarization effect is well known to degrade the energy resolution and shift the photo peaks under a continuous bias voltage applying. By removing the bias voltage and re-applying, the detector can recover to the initial state. In this study, the similar phenomenon was observed as the degradation of the spatial resolution in several tens of minutes at a continuous bias voltage of 500 V. However, it was found that momentary removal of the bias returns the spatial resolution to its initial state. We applied the periodic bias reset operation to prevent the polarization effect, where the bias-on time and the off-time were set to be 5 min and 0.5 sec, respectively. These values were consistent with those of the bias reset parameters reported in [8].

The interface board was connected to a control circuit board equipped with ADCs, a FPGA, memory ICs, regulators and Camera Link PCI interface. The ASICs were controlled by the FPGA. Output analog signals from the modules were converted to 12 bit digital signals with ADCs and they were stored temporarily. Then the data were transferred to the PC. The electronic devices on the control circuit board were shielded from X-rays irradiation by 1-mm-thick lead sheets. The ASICs were protected by the 1-mm-thick CdTe sensor which could be a good X-ray beam attenuator. Actually, we tested the radiation hardness of the hybrid using other hybrids. The measured dose rate was approximately 0.1 MR/hr with the distance from X-ray source of 2 cm at tube voltage of 120 kV and current of 300 $\mu$A. The dark signal and the gain linearity in the irradiated region were measured up to 10 hours in the operation of the periodic bias reset mode. The results showed that the dark signal slightly began to increase beyond 6 hours (the total dose was 0.6 MR). The dark signal increased by 1% of the full dynamic range after 10 hours (the total dose was 1 MR). No change of the gain linearity was observed.

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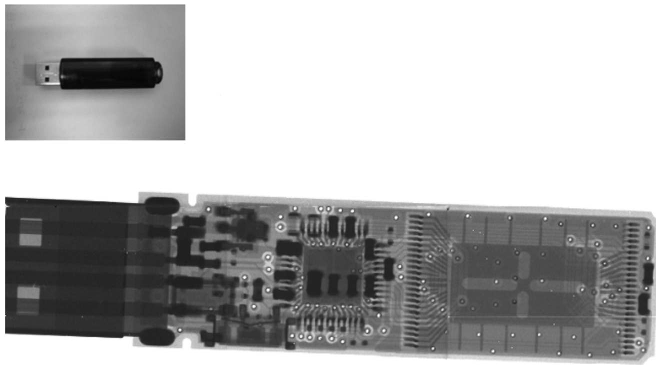

Fig. 8. X-ray image of a USB flash drive taken at 80 kV.

The uniformity of gain for the CdTe FPD was evaluated by taking a flat- field X-ray image. The proportion of dead pixels including bump failure pixels, high leakage current pixels and irregular gain linearity pixels was approximately 0.3% in one hybrid module. Both of standard deviations of gain among pixels and hybrids were less than 5%.

Fig. 8 shows an X-ray image of an USB flash drive taken by the prototype CdTe FPD at 80 kV, where the image correction was performed by adjustment of differences in the gain linearity among pixels and replacement of missing data due to the gaps with average of the neighboring pixels. The detail of the drive is clearly visible. A high resolution X-ray image was successfully obtained.

Fig. 9 shows one frame of a real time X-ray image series of a watch taken at 100 kV at 50 fps. It is the raw image without any image correction. Details of gear pairs and the fast rotating balance wheel are visible.

## IV. Conclusion

The 4-sides buttable CdTe-ASIC hybrid module for X-ray Flat Panel Detector was successfully developed by applying TSV technology. The 4-sides buttable hybrid module has the excellent spatial resolution characteristic compared with the commercially available indirect X-ray conversion type CsI(Tl) FPD. Especially, the MTF value of the CdTe module was found to be significantly higher than that of the CsI(Tl) FPD in all frequency range. The prototype CdTe FPD was made by assembling 9 pieces of the 4-sides buttable hybrid modules into 3 $\times$ 3 arrays with the 50- $\mu$m-gap among hybrids. A high resolution real time X-ray image was obtained at high frame rate of 50 fps.

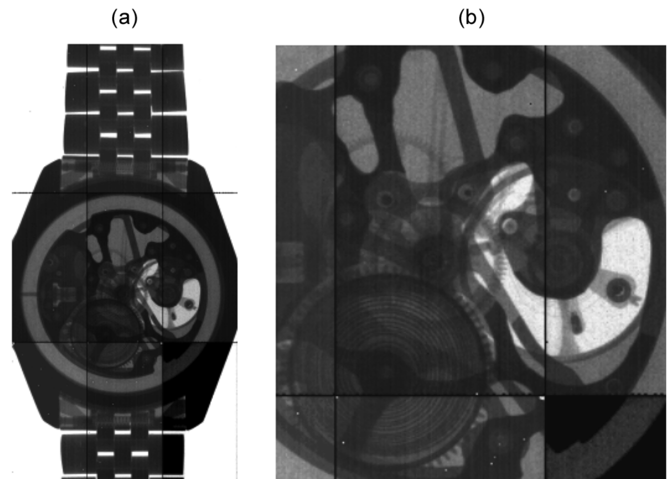


Fig. 9. (a) One frame of a real time X-ray image series of a watch taken at 100 kV at 50 fps, (b) an enlarged image of central area of the X-ray image.

These results showed the great potential of this 4-sides buttable CdTe module for a new real time X-ray FPD with high spatial resolution.

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